UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/076,415	02/19/2002	James Aweya	57983.000061	2130

7590	07/26/2005

Thomas E. Anderson
Hunton & Williams
1900 K Street, N.W.
Washington, DC 20006-1109

EXAMINER
SURYAWANSHI, SURESH

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

		Application No.	Applicant(s)
		10/076,415	AWEYA ET AL.
Office Action Summary		Examiner	Art Unit
		Suresh K. Suryawanshi	2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/13/05 amendments*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date *7/14/05*.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

1.   Claims 1-20 are presented for examination.

Claim Rejections - 35 USC § 101

2.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3.   Claims 10 and 20 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

4.   Claims are not limited to tangible embodiments. In view of applicant's disclosure, specification [page 13, lines 11-15; page 15, line 19 -- page 16, line 5; page 33, lines 4-8], the medium is not limited to tangible embodiments, instead being defined as including intangible embodiments [e.g., carrier wave or signals]. As such, the claims are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.   Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Bleiweiss et al

(US Patent No 5,970,107[1]; hereinafter Bleiweiss).

7.   As per claim 1, Bleiweiss discloses a method for synchronizing clocks in a network [col.

1, lines 31-35], the method comprising the steps of:

receiving a first timestamp and a second timestamp each indicating a respective time

instance within the network [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53

-- col. 9, line 5; col. 12, lines 46-67; time stamps of the remote clock and local clock];

measuring a first time interval between the first timestamp and the second timestamp as

determined by a first clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8,

line 53 -- col. 9, line 5; col. 12, lines 46-67; determining the slope of time stamps of the remote

clock];

---

[1] Prior art cited by applicants in the information disclosure statement (dated 7/14/05).

measuring a second time interval between the first timestamp and the second timestamp as determined by a second clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; determining the slope of time stamps of the local clock];

generating a difference signal representing a difference between the first time interval and the second time interval [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; forming the difference between the slope of the time stamps of the remote clock and the slope of the time stamps of the local clock];

filtering the difference signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; filtering the difference signal to generate a frequency adjustment signal]; and

generating the second clock signal based upon the difference signal such that the second clock signal is synchronized with the first clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; adjusting the frequency of the local clock according to the magnitude of the frequency adjustment signal].

8.   As per claim 11, Bleiweiss discloses an apparatus for synchronizing clocks in a network

[col. 1, lines 31-35], the apparatus comprising:

        a receiver for receiving a first timestamp and a second timestamp each indicating a

respective time instance within the network [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-

11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; time stamps of the remote clock and local

clock]; and

        a phase-locked loop associated with the receiver [col. 7, line 64 -- col. 8, line 1; PLL], the

phase-locked loop comprising:

        a first differencing element for measuring a first time interval between the first timestamp

and the second timestamp as determined by a first clock signal [col. 2, lines 51-59; col. 3, lines

2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; determining the slope

of time stamps of the remote clock];

        a second differencing element for measuring a second interval between the first

timestamp and the second timestamp as determined by a second clock signal [col. 2, lines 51-59;

col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67;

determining the slope of time stamps of the local clock];

a third differencing element for generating a difference signal representing a difference

between the first time interval and the second time interval [col. 2, lines 51-59; col. 3, lines 2-8;

col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; forming the difference

between the slope of the time stamps of the remote clock and the slope of the time stamps of the

local clock];

a filter for filtering the difference signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines

2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; filtering the difference signal to

generate a frequency adjustment signal]; and

a variable oscillator for generating the second clock signal based upon the filtered

difference signal such that the second clock signal is synchronized with the first clock signal

[col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12,

lines 46-67; generating the local clock according to the magnitude of the frequency adjustment

signal].

9.   As per claim 20, Bleiweiss discloses an article of manufacture for synchronizing clocks

in a network [col. 1, lines 31-35], the article of manufacture comprising:

at least one processor readable carrier [col. 5, lines 46-51; a processor executing

instructions; col. 8, lines 55-57; FIFO; col. 9, line 34 -- col. 10, line 9; executing code or

software implementation; col. 1, lines 39-53; inherent to the system]; and

instructions carried on the at least one carrier [col. 5, lines 46-51; a processor executing

instructions; col. 8, lines 55-57; FIFO; col. 9, line 34 -- col. 10, line 9; executing code or

software implementation; col. 1, lines 39-53; inherent to the system];

wherein the instructions are configured to be readable from the at least one carrier by at

least one processor [col. 5, lines 46-51; a processor executing instructions; col. 8, lines 55-57;

FIFO; col. 9, line 34 -- col. 10, line 9; execution of codes or software implementation by a

processor] and thereby cause the at least one processor to operate so as to :

receive a first timestamp and a second timestamp each indicating a respective time

instance within the network [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53

-- col. 9, line 5; col. 12, lines 46-67; time stamps of the remote clock and local clock];

measure a first time interval between the first timestamp and the second timestamp as

determined by a first clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8,

line 53 -- col. 9, line 5; col. 12, lines 46-67; determining the slope of time stamps of the remote

clock];

measure a second time interval between the first timestamp and the second timestamp as

determined by a second clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col.

8, line 53 -- col. 9, line 5; col. 12, lines 46-67; determining the slope of time stamps of the local

clock];

generate a difference signal representing a difference between the first time interval and

the second time interval [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8, line 53 --

col. 9, line 5; col. 12, lines 46-67; forming the difference between the slope of the time stamps of

the remote clock and the slope of the time stamps of the local clock];

filter the difference signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5, lines 2-11; col. 8,

line 53 -- col. 9, line 5; col. 12, lines 46-67; filtering the difference signal to generate a frequency

adjustment signal]; and

generate the second clock signal based upon the difference signal such that the second

clock signal is synchronized with the first clock signal [col. 2, lines 51-59; col. 3, lines 2-8; col.

5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; generating the local clock

according to the magnitude of the frequency adjustment signal].

10.   As per claims 2 and 12, Bleiweiss discloses delaying the first timestamp by a first delay

amount so as to measure the first time interval between the first timestamp and the second

timestamp as determined by the first clock signal [col. 5, lines 2-5; time difference between

current and previous time stamps of the remote clock].

11.   As per claims 3 and 13, Bleiweiss discloses disclose delaying the first timestamp by a

second delay amount so as to measure the second time interval between the first timestamp and

the second timestamp as determined by the second clock signal [col. 5, lines 2-5; time difference

between current and previous time stamps of the local clock].

12.   As per claims 4 and 14, Bleiweiss discloses disclose that the first delay amount and the

second delay amount are substantially equal delay amounts [col. 5, lines 2-5; clearly the first

delay amount and the second delay amount will be same when the second clock in synchronism

with the first clock].

13.   As per claims 5 and 15, Bleiweiss discloses initializing the difference signal prior to

receiving the first timestamp and the second timestamp [col. 12, lines 46-67; inherent to the

system as the difference signal will be reset prior to forming a new difference signal].

14.   As per claims 6 and 16, Bleiweiss discloses filtering the difference signal comprises

filtering the difference signal with a low pass filter such that the second clock signal is

synchronized with the first clock signal based upon the filtered difference signal [col. 12, lines

52-58; filtering the difference signal; col. 9, lines 6-10; loop filter].

15.   As per claims 7 and 17, Bleiweiss discloses disclose initializing the filtered difference

signal prior to receiving the first timestamp and the second timestamp [col. 12, lines 46-67;

inherent to the system as the filtered difference signal will be reset prior to receiving a new set of

time stamps].

16.   As per claims 8 and 18, Bleiweiss discloses controlling the period of a digitally

controlled oscillator based upon the difference signal [col. 2, lines 51-59; col. 3, lines 2-8; col. 5,

lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines 46-67; generating the local clock

according to the magnitude of the frequency adjustment signal].

17.   As per claims 9 and 19, Bleiweiss discloses converting the difference signal from a

digital difference signal value into analog difference signal value and controlling the period of a

voltage controlled oscillator based upon the analog difference signal value [col. 2, lines 51-59;

col. 3, lines 40-43; an analog PLL; col. 5, lines 2-11; col. 8, line 53 -- col. 9, line 5; col. 12, lines

46-67; generating the local clock according to the magnitude of the frequency adjustment signal].

18.   As per claim 10, Bleiweiss discloses a computer signal embodied in a carrier wave

readable by a computing system and encoding a computer program of instructions for executing

a computer process performing the method recited in claim 1 [col. 5, lines 46-51; a processor

executing instructions; col. 8, lines 55-57; FIFO; col. 9, line 34 -- col. 10, line 9; executing code

or software implementation; col. 1, lines 39-53; inherent to the system].

Response to Arguments

19.   Applicant's arguments with respect to claims 1-20 have been considered but are moot in

view of the new ground(s) of rejection.
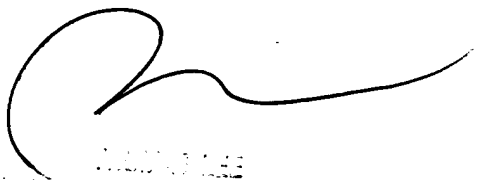
Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Suresh K. Suryawanshi whose telephone number is 571-272-

3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
July 19, 2005